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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,812	03/22/2004	Raul Alejandro Perez	TI-36957	1062

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,812	PEREZ, RAUL ALEJANDRO	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-14 and 16-20* is/are rejected.

7)☒ Claim(s) *9 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 8/31/05. A new ground of rejection is introduced as necessitated by amendment.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 is indefinite because it is unclear why the impedance of the first node is higher than it self's impedance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3, 4, 6-8, 10, 11, 19 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Noda et al. (US 2004/0080352).

As to claim 1, Noda et al.'s figure 1 shows a method of stabilizing two current loops within a circuit comprising the steps of: providing a main current loop (the lower loop 19) for

supplying current to a load (Ra); providing a sensing loop (upper loop 8) for controlling the current to the load; an error amplifier (all elements in 19) for the main current loop coupled to the output of an error amplifier (all elements in 18) for the sensing loop such that the capacitance of each loop is isolated from that of the other loop; and providing a compensating capacitor (C11, C12) to each loop whereby stability is independently maintained for each loop within selected operational criteria.

As to claims 3 and 4, figure 1 shows that the output of the main loop error amplifier comprises a first node (n4) having a higher impedance than a second node (source of Q34), the compensating capacitor being coupled to the second node.

As to claim 6, figure 1 shows a circuit having a low capacitive load and comprising two stable current loop sub circuits (18, 19) further comprising: a main current loop (18) for supplying current to the load, the main current loop having a first compensation capacitor (C12) for maintaining stability within a pre-selected operational range; a sensing loop (19 except Q11) for controlling the current to the load, the sensing loop having a send compensation capacitor (C11) for maintaining stability within a pre-selected operational range; and a transistor (Q11) for coupling the output of the main current loop error amplifier and the output of the sensing loop such that the first compensation capacitor is isolated from the second compensation capacitor.

As to claim 7, figure 1 shows that the transistor comprises a MOSFET.

As to claim 8, figure 1 shows that the transistor comprises a bipolar transistor (paragraph [0068]).

As to claim 10, figure 1 shows that the main loop further comprises a main load error amplifier (Q29-Q33) having a plurality of output nodes (node between 32 and 29 and node

between 33 and 30) and wherein the output of the main loop error amplifier comprises lower impedance node (lower than the source of Q33) of the error amplifier.

As to claim 11, figure 1 shows that the output of the main loop comprises a higher impedance node (higher than the source of Q30) of the error amplifier.

As to claims 19 and 20, figure 1 shows that the sensing loop limits the maximum current to the load.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (USP 6806692) in view of Larson et al. (USP 6201375).

As to claim 1, Lee's figure 2 shows a method comprising the steps of: providing a main current loop (COMP2, P2, R1, R2) for supplying current to a load (not shown); providing a sensing loop (COMP1, P1, P3) for controlling the current to the load; an error amplifier (COM2, P2) for the main current loop coupled to the output of an error amplifier (COM1, P1) for the sensing loop such that the capacitance of each loop is isolated from that of the other loop; and providing a compensating capacitor (Pcc) for the sense loop. Thus, figure 2 shows all limitations of the claim except for the step of providing compensating capacitor for the main loop. However, Larson et al.'s figure 2 shows a circuit having compensating capacitor Cout coupled to the output of the main loop in order to stabilize the output voltage. Therefore, it would have

been obvious to one having ordinary skill in the art to add a compensating capacitor to the output of Lee's main loop for the purpose of stabilizing the output voltage.

As to claim 2, Lee's figure 2 shows the step of coupling the output of the error amplifier to the gate of a transistor (P3) and coupling the compensating capacitor (Pcc) of the sensing loop to the source of the transistor.

As to claims 3 and 4, Lee's figure 2 shows that the output of the main loop error amplifier (COMP2) comprises a first node having a higher impedance than a second node (Vdd node) the compensating capacitor being coupled to the second node.

As to claim 5, Lee's figure 2 shows that the main loop comprises a low dropout regulator (LDO).

As to claim 19, figure 2 shows that the sensing loop limits the maximum current to the load.

7. Claims 5, 12, 13, 14 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noda et al. (US 20040080352).

As to claims 5 and 12, Noda et al. fails to teach that the main loop comprises low dropout (LDO) voltage regulator. However, it is notoriously well known in the art that LDO voltage regulator proving stable supply voltage. Therefore, it would have been obvious to one having ordinary skill in the art to use LDO voltage regulator as a supply circuit for supplying VDD to the main loop for the purpose of operating the circuit figure 11 precisely.

As to claims 13, 14, 16 and 17 Noda et al.'s figure 1 shows all limitations of the claim except for 1 μF load capacitance. However, it is well known in the art that load capacitor is for filtering unwanted noise, the it is seen as a design preference to select particular value for the

load capacitor dependent upon particular environment of use to ensure optimum performance. Therefore, it would have been obvious to one having ordinary skill in the art to use 1μF capacitor coupled to the output of circuit 11 for the purpose of reducing noise.

As to claim 18, it is seen as an intended use for using the circuit in a LDO voltage regulator.

Allowable Subject Matter

8. Claims 9 and 15 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 9 and 15 would be allowable because the prior art fails to teach or suggest that the output of the main current loop error amplifier is coupled to the gate of the transistor and me output of the sensing loop error amplifier is coupled to the source of the transistor via the second compensation capacitor.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

October 28, 2005